Eternal Semiconductor Inc.

ET080N08T

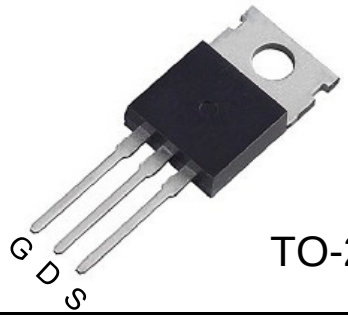
N-Channel Enhancement-Mode MOSFET (80V, 80A)

PRODUCT SUMMARY

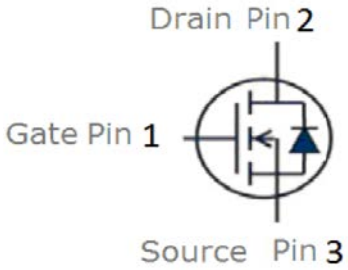
V_{DSS}	I_D	$R_{DS(on)}$ (mΩ) Typ
80	80	6.8@ VGS = 10V, ID=40A

Features

- Super high density cell design for extremely low RDS(ON)
- Exceptional on-resistance and maximum DC current capability
- 100% Avalanche test
- Lead（Pb）-free and halogen-free



TO-220



Pin 1 : Gate
Pin 2: Drain
Pin 3: Source

Absolute Maximum Ratings (T_A=25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	80	V
V_{GS}	Gate-Source Voltage	±25	V
I_D	Drain Current (Continuous)@TA=25°C	80	A
	Drain Current (Continuous)@TA=75°C	60	A
I_{DM}	Drain Current (Pulsed) [a]	180	A
P_D	Total Power Dissipation @T_A=25°C	150	W
	Total Power Dissipation @T_A=75°C	90	W
E_{AS}	Avalanche Energy,Single Pulsed,L=0.5mH	540	mJ
I_S	Maximum Diode Forward Current	80	A
T_j, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +150	°C
R_{QJA}	Thermal Resistance Junction to Ambient (PCB mounted)[b]	40	°C/W

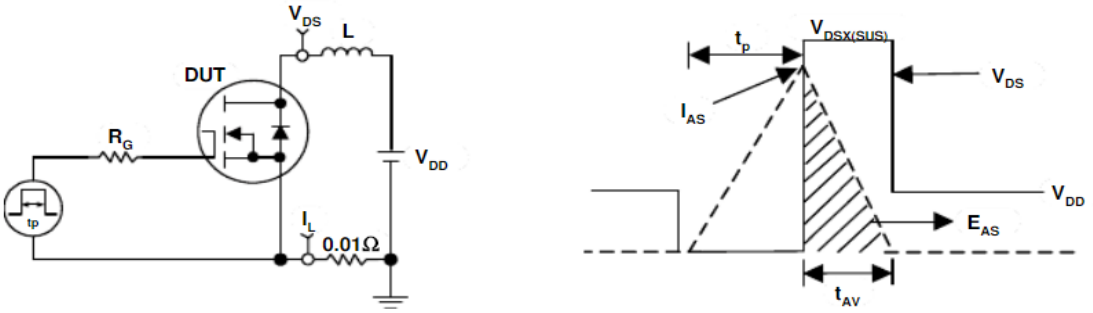
a: Repetitive Rating: Pulse width limited by the maximum junction temperature.

b: 1-in^2 2oz Cu PCB board

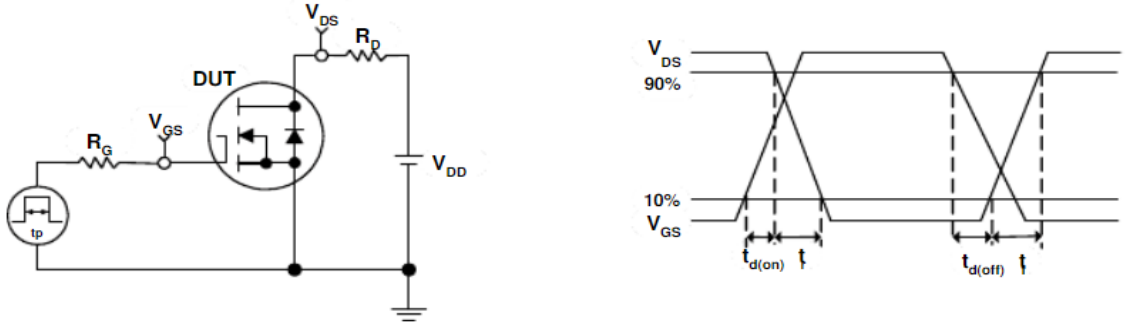
Electrical Characteristics (T_A=25°C, unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
• Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	80	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0V	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±25V, V_{DS}=0V	-	-	±100	nA
• On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2.0	3.0	4.0	V
$R_{DS(on)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=40A	-	6.8	8	mΩ
• Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=30V, V_{GS}=0V, f=1MHz	-	2820	-	PF
C_{oss}	Output Capacitance		-	390	-	
C_{rss}	Reverse Transfer Capacitance		-	255	-	
• Switching Characteristics						
Q_g	Total Gate Charge	V_{DS}=40V, I_D=30A, V_{GS}=10V	-	88	-	nC
Q_{gs}	Gate-Source Charge		-	18	-	
Q_{gd}	Gate-Drain Charge		-	29	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=30V, R_L=15Ω, I_D=40A, V_{GEN}=10V, RG=6Ω	-	17	-	nS
t_r	Turn-on Rise Time		-	69	-	
$t_{d(off)}$	Turn-off Delay Time		-	50	-	
t_f	Turn-off Fall Time		-	73	-	
• Drain-Source Diode Characteristics						
V_{SD}	Drain-Source Diode Forward	V_{GS}=0V, I_S=40A	-	-	1.2	V

Note: Pulse Test: Pulse Width≤300us, Duty Cycle≤2%



Avalanche Test Circuit and Waveforms



Avalanche Test Circuit and Waveforms

Typical Characteristics Curves (Ta=25°C, unless otherwise note)

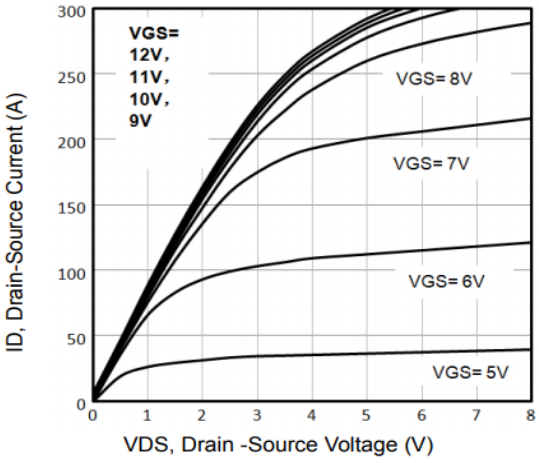


Fig1. Typical Output Characteristics

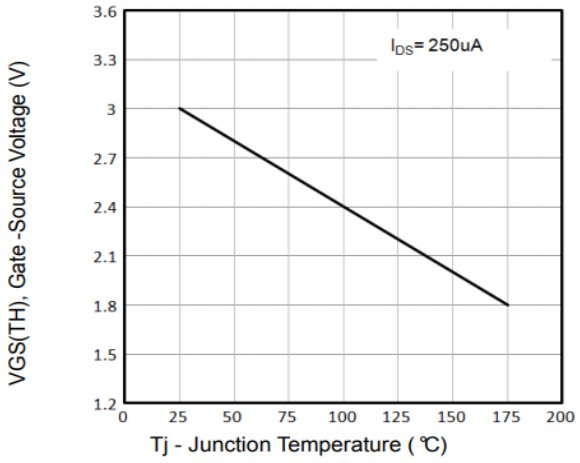


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

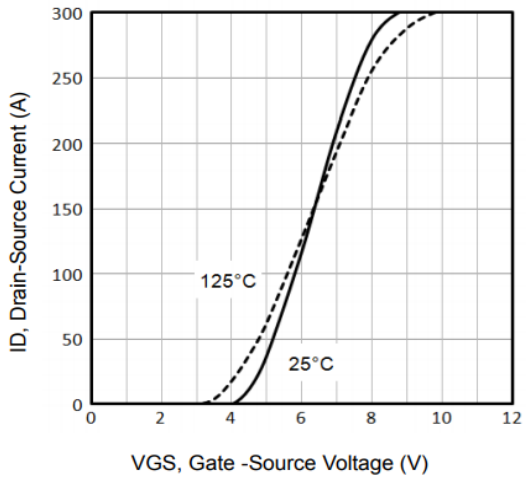


Fig3. Typical Transfer Characteristics

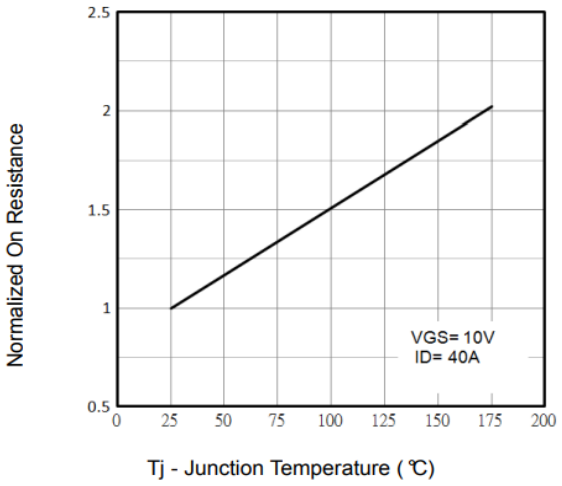


Fig4. Normalized On-Resistance Vs. Tj

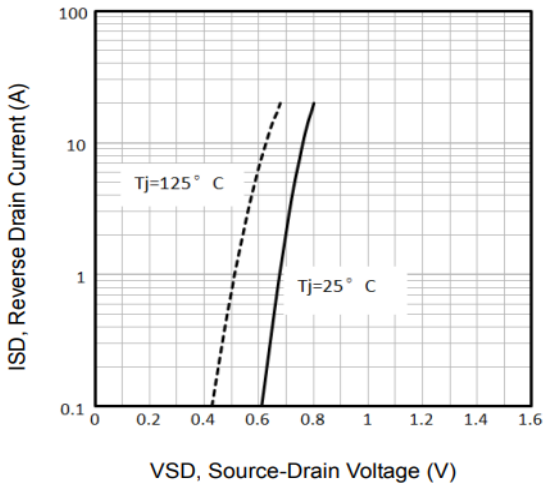


Fig5. Typical Source-Drain Diode Forward Voltage

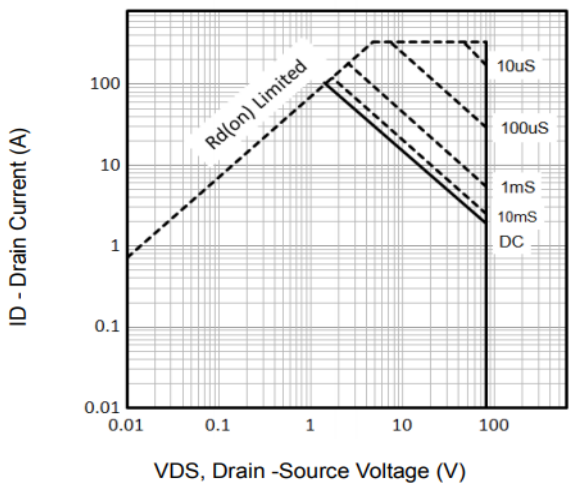


Fig6. Maximum Safe Operating Area

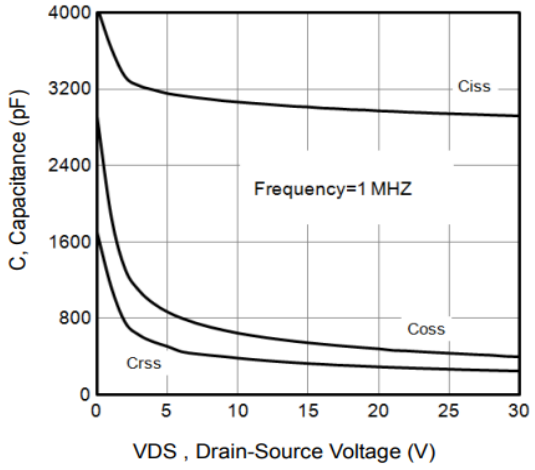


Fig7. Typical Capacitance Vs.Drain-Source Voltage

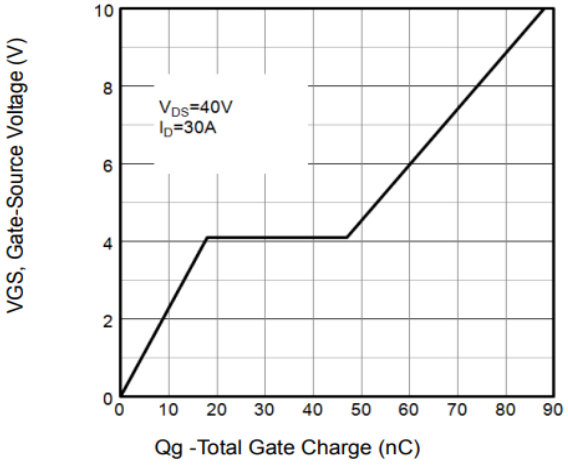


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

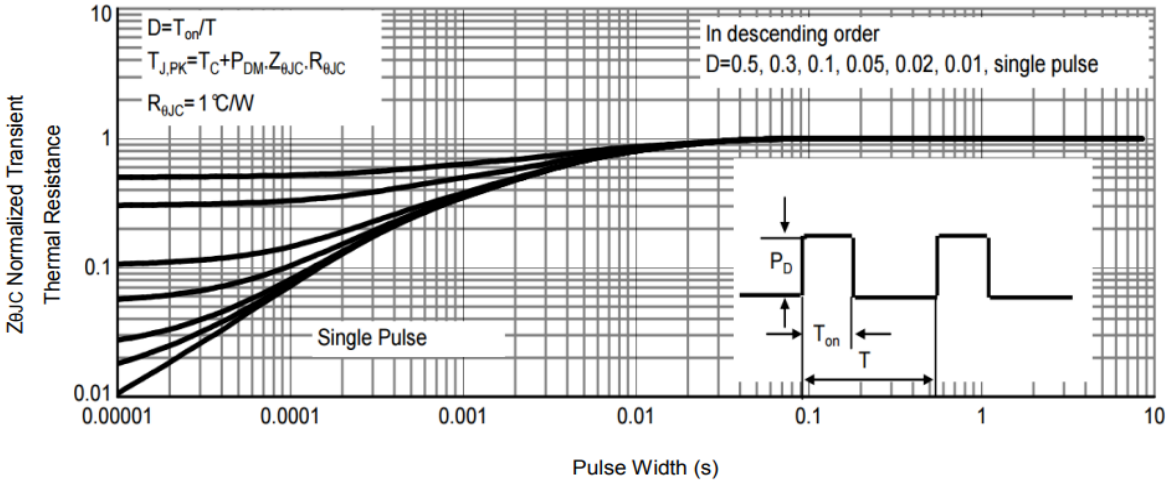
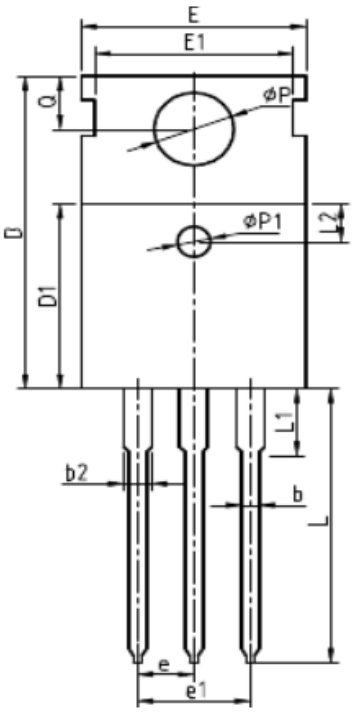
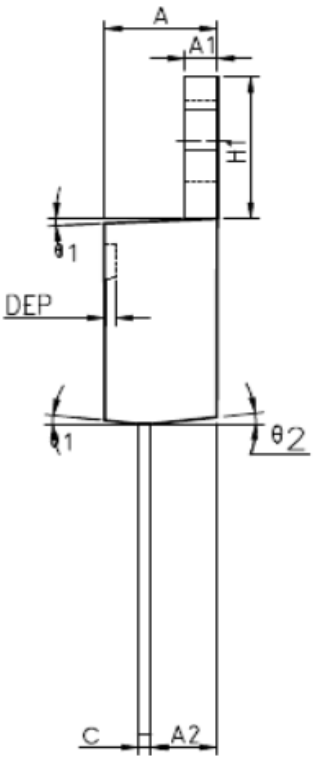
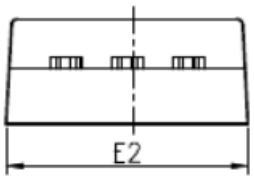


Fig9. Normalized Maximum Transient Thermal Impedance

TO-220-3L PACKAGE OUTLINE DIMENSIONS







COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.33	0.050	0.051	0.052
A2	2.35	2.40	2.50	0.093	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	-	8.70	-	-	0.343	-
E2	9.80	10.00	10.20	0.386	0.394	0.402
e		2.54	BSC		0.100	BSC
e1		5.08	BSC		0.200	BSC
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	-	3.10	3.30	-	0.122	0.130
L2		2.50	REF		0.098	REF
P	3.50	3.60	3.63	0.138	0.142	0.143
P1	3.50	3.60	3.63	0.138	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.113
θ1	5°	7°	9°	5°	7°	9°
θ2	1°	3°	5°	1°	3°	5°
θ3	1°	3°	5°	1°	3°	5°