



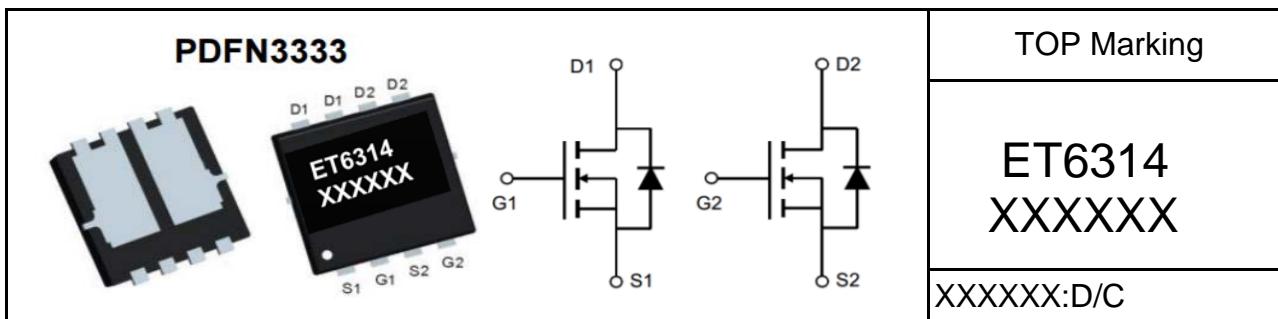
Dual N-Channel High Density Trench MOSFET (30V,28A)

PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (mΩ) Typ.
30V	28A	9 @ VGS = 10V, ID=20A
		12@ VGS = 4.5V, ID=10A

Features

- Super high density cell design for extremely low RDS(ON)
- Exceptional on-resistance and maximum DC current capability
- Lead (Pb) -free and halogen-free



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current (Continuous)@ $T_A=25^\circ\text{C}$	28	A
	Drain Current (Continuous)@ $T_A=75^\circ\text{C}$	18	A
I_{DM}	Drain Current (Pulsed) ^a	92	A
P_D	Total Power Dissipation @ $T_A=25^\circ\text{C}$	14	W
	Total Power Dissipation @ $T_A=75^\circ\text{C}$	7	W
EAS	Avalanche energy, single pulsed	18	Mj
I_S	Maximum Diode Forward Current	28	A
T_j, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +150	°C
R_{QJA}	Thermal Resistance Junction to Ambient (PCB mounted) ^b	45	°C/W

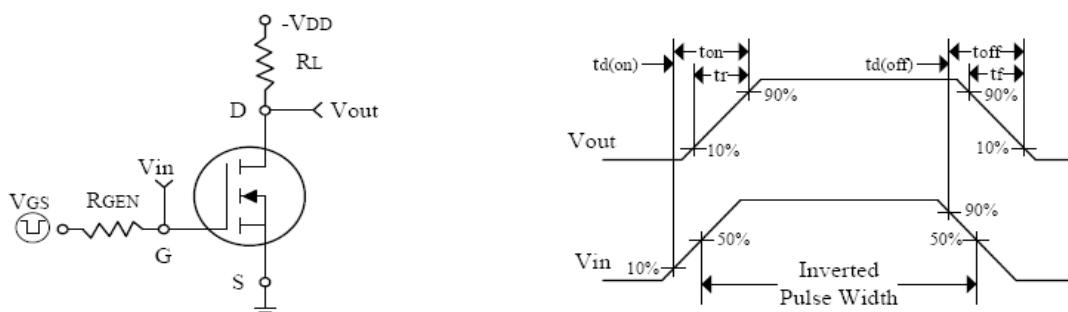
a: Repetitive Rating: Pulse width limited by the maximum junction temperature.

b: 1-in² 2oz Cu PCB board

Electrical Characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
• Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
• On Characteristics						
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.0	1.9	2.5	V
$R_{\text{DS}(\text{on})}$	Drain-Source On-State Resistance	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$	-	9	13	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=10\text{A}$	-	12	18	
• Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	-	860	-	PF
C_{oss}	Output Capacitance		-	140	-	
C_{rss}	Reverse Transfer Capacitance		-	105	-	
• Switching Characteristics						
Q_g	Total Gate Charge	$V_{\text{DS}}=15\text{V}, I_{\text{D}}=20\text{A}, V_{\text{GS}}=10\text{V}$	-	19	-	nC
Q_{gs}	Gate-Source Charge		-	4.3	-	
Q_{gd}	Gate-Drain Charge		-	6.5	-	
$t_{\text{d}(\text{on})}$	Turn-on Delay Time	$V_{\text{DD}}=15\text{V}, R_L=15\Omega, I_{\text{D}}=20\text{A}, V_{\text{GEN}}=10\text{V}, R_G=6\Omega$	-	6	-	nS
t_r	Turn-on Rise Time		-	5	-	
$t_{\text{d}(\text{off})}$	Turn-off Delay Time		-	25	-	
t_f	Turn-off Fall Time		-	7	-	
• Drain-Source Diode Characteristics						
V_{SD}	Drain-Source Diode Forward	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=20\text{A}$	-	-	1.2	V

Note: Pulse Test: Pulse Width $\leq 300\text{us}$, Duty Cycle $\leq 2\%$



Switching Test Circuit and Switching Waveforms

Typical Characteristics Curves (Ta=25°C, unless otherwise note)

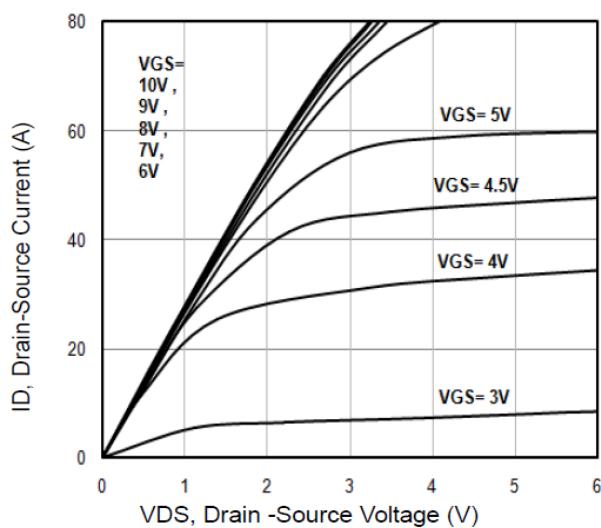


Fig1. Typical Output Characteristics

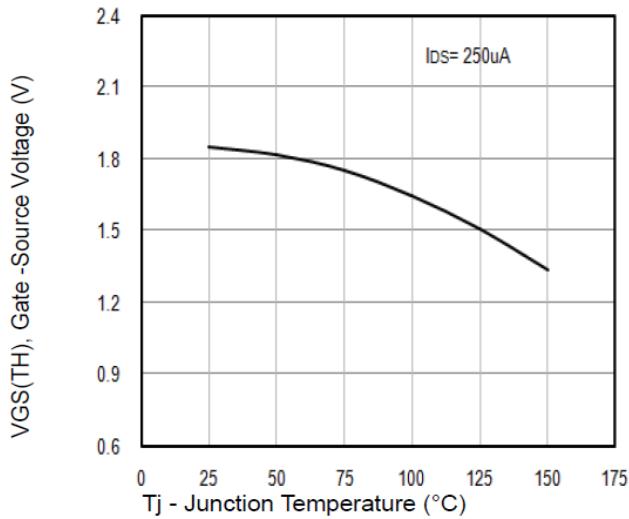


Fig2. $VGS(TH)$ Gate -Source Voltage Vs. T_j

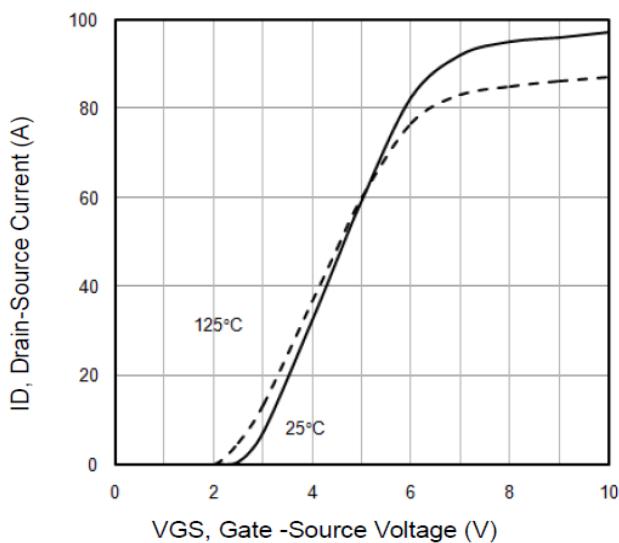


Fig3. Typical Transfer Characteristics

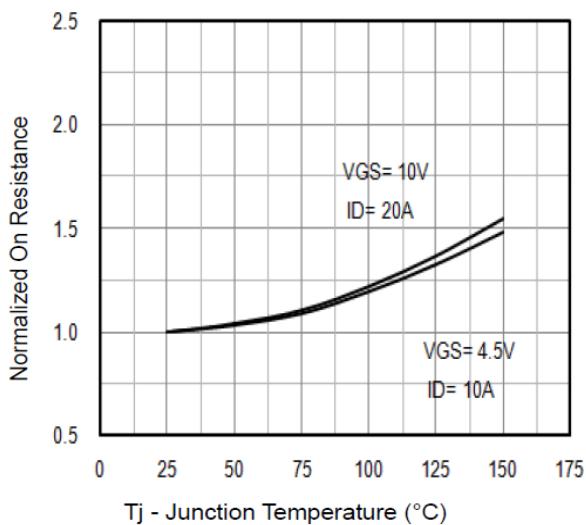


Fig4. Normalized On-Resistance Vs. T_j

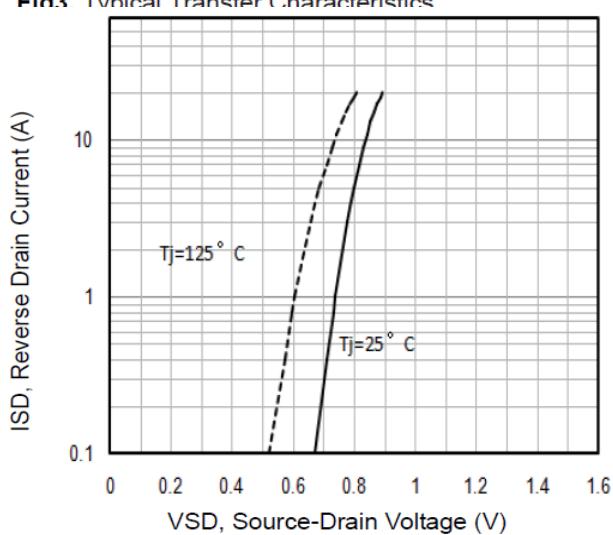


Fig5. Typical Source-Drain Diode Forward Voltage

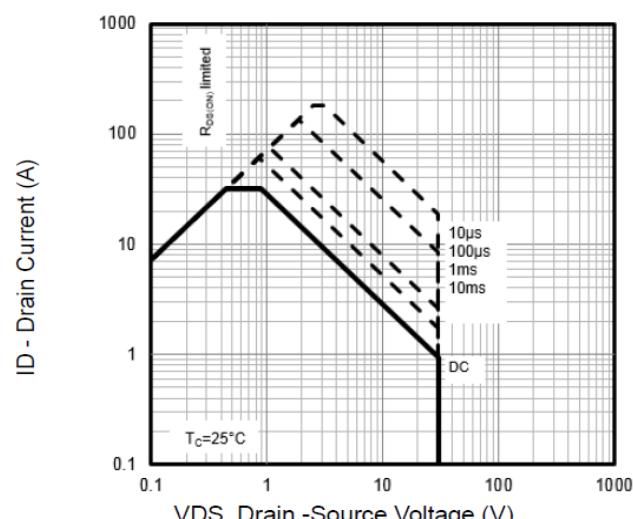


Fig6. Maximum Safe Operating Area

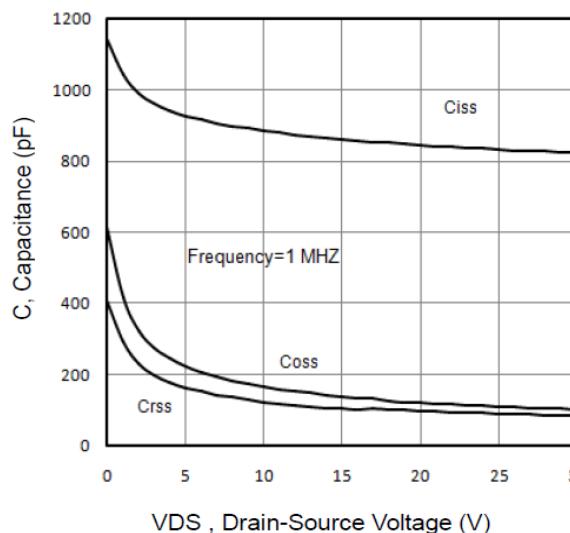


Fig7. Typical Capacitance Vs.Drain-Source Voltage

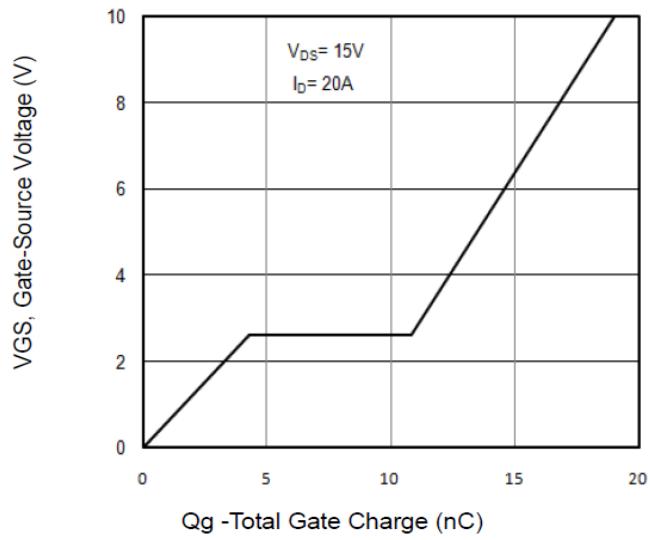


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

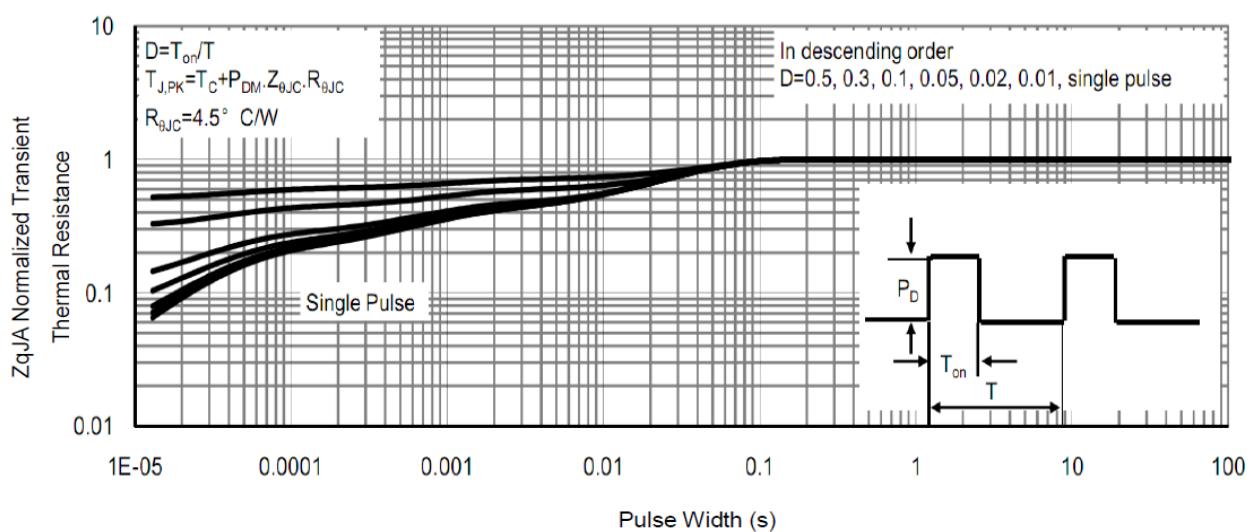


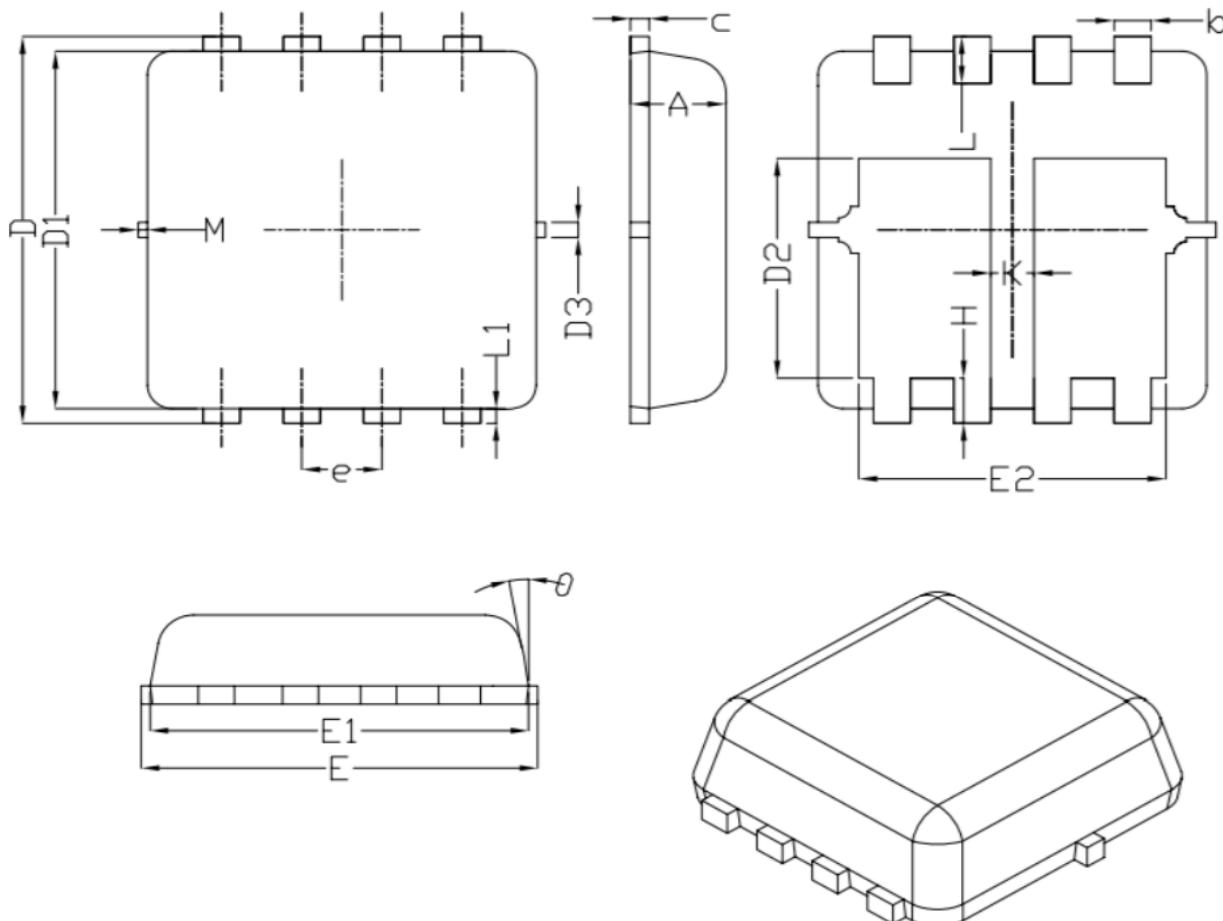
Fig9. Normalized Maximum Transient Thermal Impedance



Eternal Semiconductor Inc.

ET6314

Dual PDFN3333 Package Outline Data



Symbol	Dimensions (unit : mm)		
	Min	TYP	Max
A	0.70	0.75	0.8
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.2
D2	1.78	1.88	1.98
D3	-	0.13	-
E	3.20	3.30	3.4
E1	3.00	3.15	3.2
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.5
L	0.30	0.40	0.5
L1	-	0.13	-
K	0.30	-	-
θ	-	10°	12°
M	*	*	0.15